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Performance Evaluation of Fully Depleted Silicon on Insulator MOSFET

Yogendra Kumar Sharma[1], Imran Ullah Khan[2]

[1, 2] Department of ECE, Integral University, Lucknow, India.

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***Abstract*— VLSI technology development nowadays is mostly focused on the downsizing of semiconductor devices, which is significantly reliant on advancements in complementary metal-oxide-semiconductor technology. Due to capacitance, shorter channel length, body biassing, faster-switching transistor, limited variability, and faster running transistor, Silicon-on-Insulator technology has seen a lot of changes. In comparison to traditional bulk technology, Silicon on Insulator offers intriguing new possibilities. The recent stalling of advancement in CMOS technology has been noticed. A fully depleted silicon on the insulator provides additional performance. Power usage and communication speed are two areas where performance can be improved. Silicon on insulator technology has the potential to reduce power consumption by nearly half while increasing speed by about 40%. Using the Atlas module of the SILVACO software, the research presents a comprehensive analysis of silicon on insulator-based nano metal oxide semiconductor field-effect transistors. Atlas is used to virtually construct a 20 nm silicon on insulator MOSFET. The gate metals employed are Aluminum, N. poly, W (Tungsten), and WSi2 (Tungsten Silicide), and their respective characteristics are obtained and compared. Finally, WSi2 was chosen as the final gate metal because it has the desired band offset, resulting in a positive threshold voltage without the need for any further implants in the channel region. Other metrics are collected, such as the variation of I_D vs. V_{GS} features at various values. There is also a fluctuation in drain current as a function of drain to source voltage.**

Keywords- MOSFET, Fully-depleted Silicon on Insulator, SILVACO, Tungsten Silicide.

I. INTRODUCTION

For several years, the semiconductor industry has seen an exponential increase in the number of transistors per IC. Predicted by Moore's law. The advancement of silicon-based CMOS technology has aided the evolution of electronics, IT, and communication. The scaling of its dimensions allows for ongoing progress. CMOS scaling is the main driving factor of Silicon technology innovation, as it improves both device density and performance. Figures 1, 2, 3, 4, 5, and 6 are representing MOSFET, SoIMOSFET, PD/FD SoIMOSFET, and different Gate structures in reference to FDSoI.

A semiconductor layer, such as germanium, is structured over a protector layer, which might be a covered oxide layer framed on a semiconductor substrate in an SoI MOSFET.

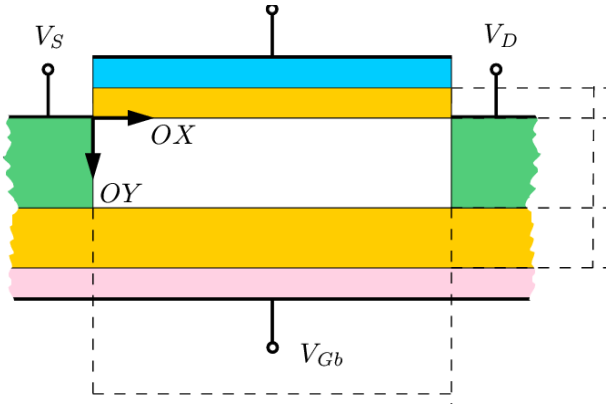

Figure 1. Idealized Geometry of the SoI MOSFET [1]

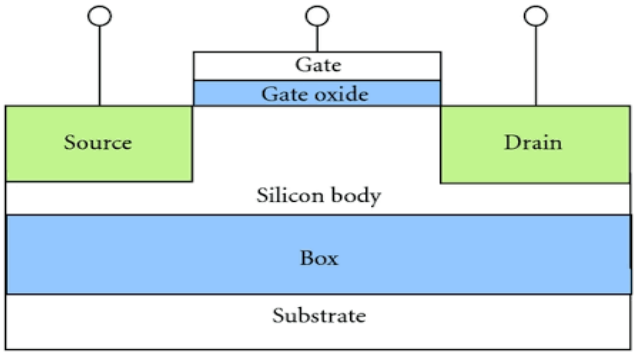

Figure 2. SoI MOSFET Structure [1]

There are two kinds of silicon on encasing MOSFET namely partially depleted and Fully Depleted abbreviated as PD and FD SoI MOSFET.

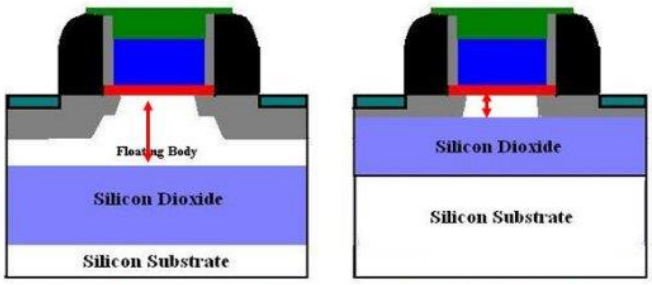

Figure 3. Partially Depleted and Fully Depleted SoI MOSFET [2]

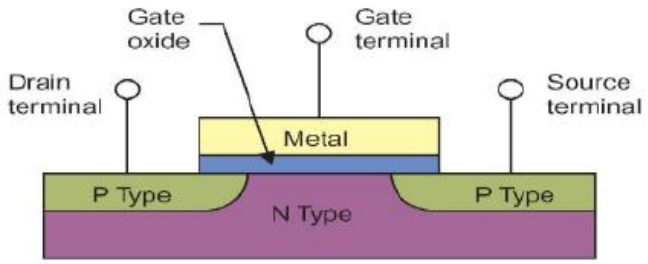

Figure 4. Cross-Sectional MOSFET [2]

The fundamental device conditions of PD SoI MOSFETs are the same concerning mass devices [1-5], with the exception of obviously the intricacies emerging from the drifting body (FBE).

II. FDSOIMOSFET

During device operation, the front and back channels of the FDSOI are electrostatically linked. The front channel FDSOI characteristics, such as channel current, edge voltage, sub-limit inclination, and so on, are subject to the back gate Voltage due to this electrostatic interaction.

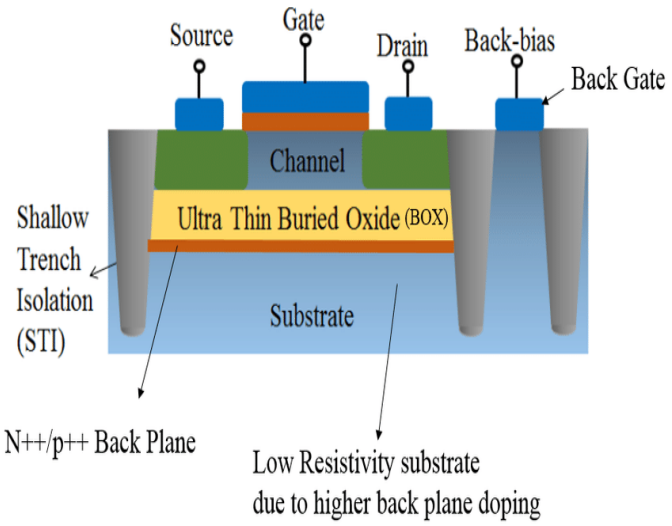

Figure 5. Fully Depleted SOI MOSFET [3]

A. *MOSFET Scaling*

For a multitude of reasons, MOSFET miniaturization is very desirable. The first and most important reason for reducing transistor sizes is to put more devices onto a single chip. As a result, the chip can perform more tasks in the same amount of area. The cost per integrated circuit is determined by the number of chips that may be produced per wafer. As a result, reducing ICs enables more chips per wafer, cutting chip prices. The number of transistors per chip has doubled every 23 years during the previous 30 years when a new technology is introduced. A CPU manufactured in 45nm technology, for example, will have double the amount of MOSFETs [7-9].

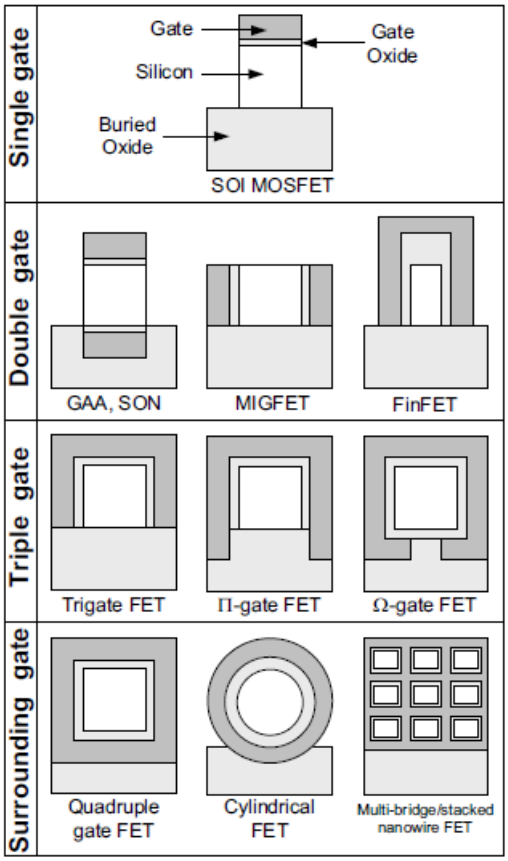

Figure 6. Different Gate Structures about FDSOI

B. *Moore's Law*

In the year 1965, Gordon Moore made a tremendous and vital observation according which every 18 or 24 months or so the number of devices on a chip gets doubled. Moore's law shows continuous miniaturization. A new technology node is introduced or a new technology generation is introduced with the reduction of minimum line width. Some of the examples of the technology generation or technology node are shown in Table I.

TABLE I. IMPROVEMENT IN TECHNOLOGY NODE OVER THE YEARS

Year	2004	2006	2008	2010	2011	2013	2016	2022
Technology Node	90 nm	65 nm	45 nm	32 nm	22 nm	16 nm	14 nm	10 nm

III. NEED OF SILICON ON INSULATOR

To improve the user experience and produce better digital devices, transistor sizes must be reduced while performance and power consumption are increased. The gate length decreases as the transistor shrinks. The transistor's control over the channel region is likewise diminished, decreasing its performance. Even when the transistor is turned off, some undesirable leakage current occurs [8, 9]. To reduce leakage current while still delivering a high-performance bulk Silicon

transistor, manufacturers have become increasingly complicated, adding new levels of manufacturing complexity at an increasing rate. In terms of technology, a new 20nm solution is required to minimize complexity while delivering the industry-expected benefits of reduced silicon geometry.

A. Shorter Channel Length

The below figure clearly described the channel length modulation effect. Long and short channel NMOS is shown in Figure 7, it can be observed that for the long channel I_{DS} is saturated after a certain voltage and for the short channel it goes on increasing.

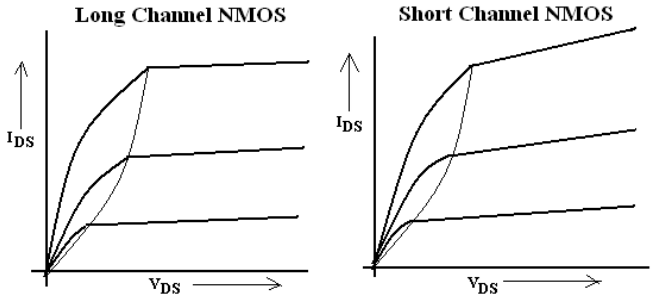

Figure 7. Effect of Channel Length Modulation [5]

B. Body Biasing and Faster Switching Transistor

The biasing creates a buried gate below the channel making the SOI act like a vertical double-gate transistor. In bulk technology, the ability to do body biasing is very limited due to parasitic current leakage. The buried gate in the SOI transistor prevents any leakage in the substrate. This allows a much higher voltage on the body leading to a significant boost in the performance. In a chip there are billions of transistors characteristics of each transistor are not exactly because the different quantities of dopants injected into the channel during the manufacturing process are the same [10-15].

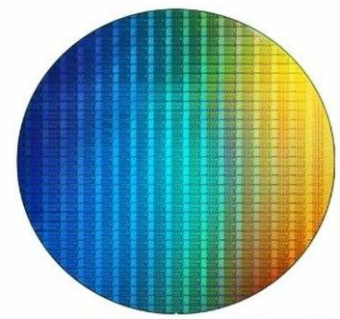

Figure 8. SOI Wafer [6]

In SOI, (shown in Figure 8) dopants usage is greatly reduced thereby limiting the variability resulting in the characteristics of each transistor being close to average in the process. This allows the transistor runs faster for a given voltage. SOI chip is able to operate at lower voltage and delivers the same performance. SOI is attractive with lower power consumption.

IV. METHODOLOGY

This chapter focuses on Silvaco Atlas software Silvaco is the short form Silicon Valley Company that is considered as one of the pioneering vendors in technology computer-aided design known as TCAD. It was established in 1984. Its headquarter is in Santa Clara, California, USA. The ability to accurately simulate a semiconductor device is somehow critical to the industry and research arena. In Silvaco, the Atlas device simulator is specially designed for 2d and 3d modeling with the ability to include electrical, optical, and thermal properties within a semiconductor device. An integrated platform based on physics is provided by Atlas to analyze DC, AC, and also time-domain responses for all semiconductor-based technologies [20].

In order to run the ATLAS in the DeckBuild, one must call the ATLAS simulator first. The command for calling the ATLAS simulator is:

go atlas

ATHENA and DevEdit are two other types of simulation software that can be used with Deck Build. Here in our work, we have used SILVACO ATLAS only.

A. Commands Atlas

After calling ATLAS, a syntax structure is to follow so that the ATLAS could execute the command file successfully. Table II shows the primary group list and statement structure specifications. The basic format of the input file statement is:

<STATEMENT><PARAMETERS>=<VALUE>

TABLE II. ATLAS COMMAND GROUPS WITH PRIMARY STATEMENTS IN EACH GROUP [24, 25]

Group	Statements
Structure Specification	MESH, REGION, ELECTRODE, DOPING
Material Models specification	MATERIAL, MODEL, CONTACT, INTERFACE
Numerical Method Selection	METHOD
Solution Specification	LOG, SOLVE, LOAD, SAVE
Results Analysis	EXTRACT, TONYPLOT

B. Structure Specification

In an inverted 2D or 3D Cartesian grid, the Mesh statement is used to define the structure. From left to right, the x-axis is positive; from bottom to top, the y-axis is negative. The inverted y-axis is due to the fact that manufacturing coordinates are typically expressed as depth below the surface. The spacing is used to refine the sharpness and precision at a given position, and all coordinates are entered in microns. Based on the user input settings, ATLAS generates a series of triangles to construct the. This command is used to mesh:

Figure 9 depicts one of the meshing, Figures 10 and 11 show SOIMOSFET 20nm complete structure and FDSOINMOSFET simulated structure. The first statement:

MESH SPACE.MULT=<VALUE>

This is followed by a series of X.MESH and Y.MESH statements:

X.MESH LOCATION=<VALUE> SPACING=<VALUE>

Y.MESH LOCATION=<VALUE> SPACING=<VALUE>

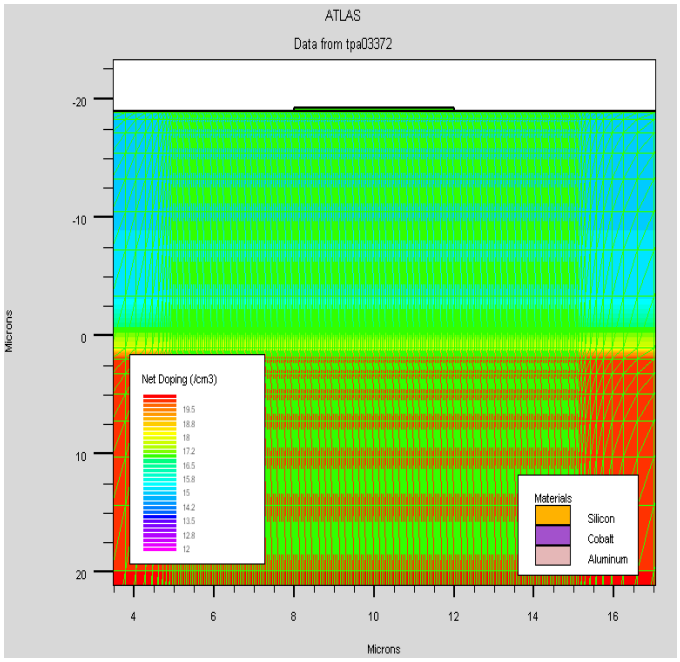

Figure 9. The Meshing of Semiconductor Device

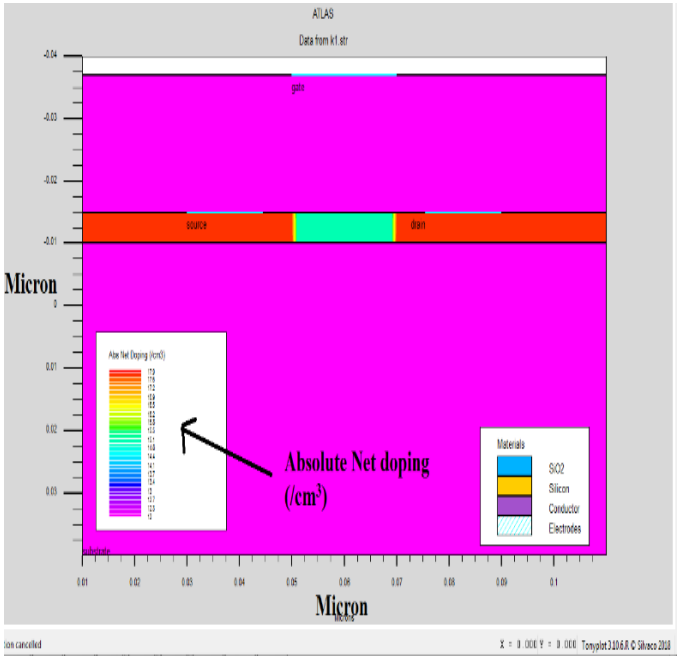

Figure 10. The Complete Structure of 20 nm SOI MOSFET

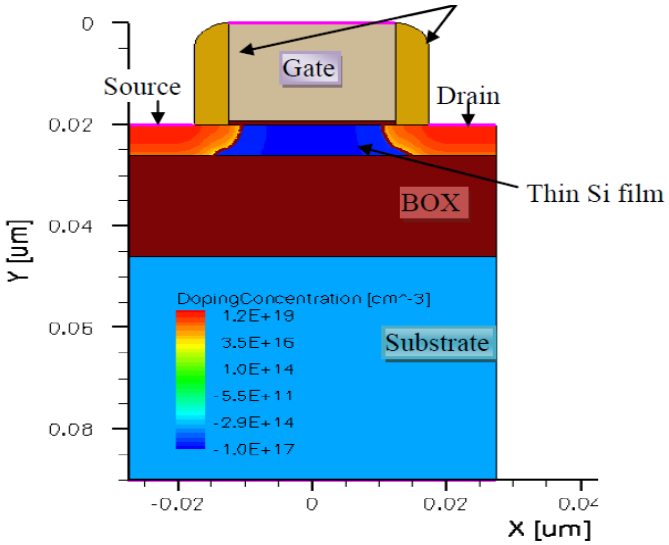

Figure 11. FDSOINMOSFET Simulated Structure [26]

V. METAL SELECTION

Four different materials have been considered Aluminum, N.poly, W (Tungsten), and WSi2 (Tungsten Silicide). I_D-V_{GS} curves have been extracted using ATLAS and graphs are shown below in Figure 12. It is clear that when Aluminum and N.poly metal are used there is negative threshold voltage is found at VT=-0.560018 V and VT=-0.394561 V, respectively. So, in this situation, we need another material that gives a positive threshold voltage. So, we move on to the W (Tungsten), and WSi2 (Tungsten Silicide), and when we used this material we got a positive threshold voltage, VT=0.912903 V and 0.025342 V, respectively. Table III represents Simulated threshold voltages of different gate metals.

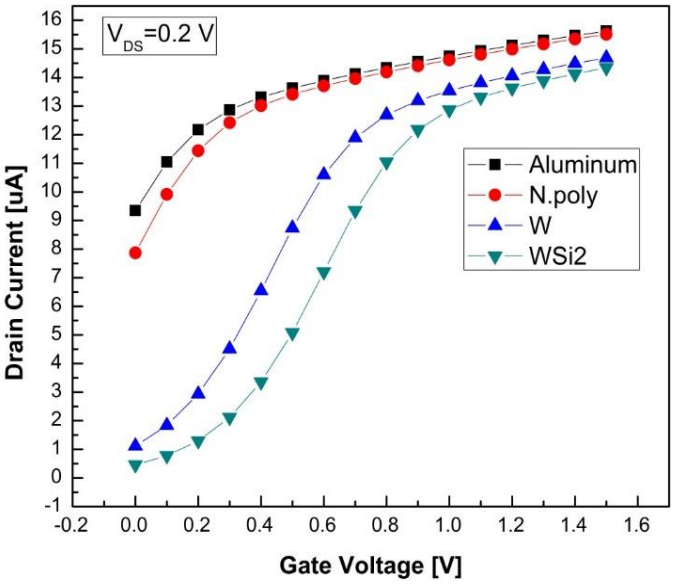

Figure 12. I_D-V_{GS} Curves for Different Metals N.poly, Aluminium, W (Tungsten), and WSi2 (Tungsten Silicide)

TABLE III. SIMULATED THRESHOLD VOLTAGES OF DIFFERENT GATE METALS

Metal	The threshold voltage (V)	Subthreshold Voltage (V/decade)
N. Poly	-0.394561	0.996183
Aluminum	-0.560018	1.37839
W (Tungsten)	0.0912903	0.462334
WSi_2 (Tungsten Silicide)	0.253420	0.435528

A. I_D versus V_{GS} Characteristics

Figure 13 shows the variation of drain current at the different drain to source voltage. From the figure, it can be observed that as a drain to source voltage increases drains current is also increasing respectively.

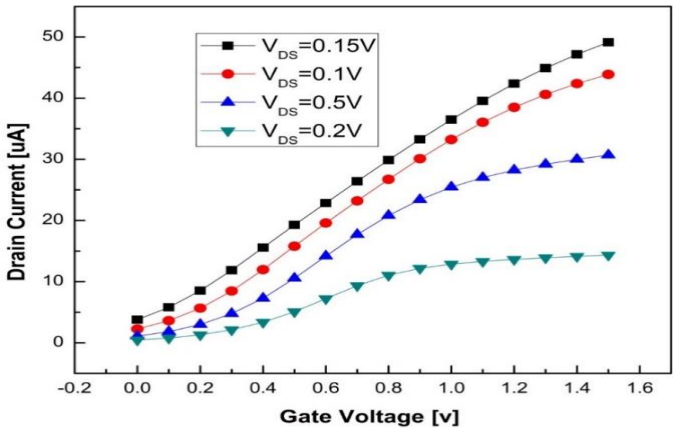

Figure 13. I_D Vs. V_{GS} Curves

B. Variation of I_D as Function of V_{DS}

Figure 14 indicates the families of I_D vs V_{DS} curves for SOI MOSFET. The plot of drain current with respect to gate voltage V_{GS}=0.7 V, 0.1 V, and 1.5 V of SOI MOSFET and V_D varying from 0 V to 1.5 V. As expected, it has been observed that the drain current increases with the increase of drain to source voltage.

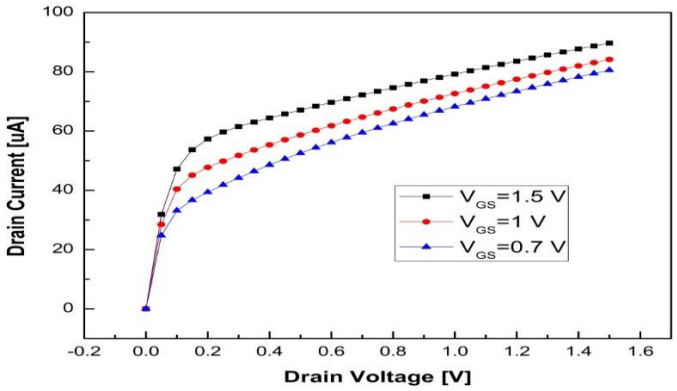

Figure 14. I_D Vs. V_{DS} Curve

VI. CONCLUSION

The bulk Si MOSFET has been the principal gadget shaping the foundation of the improvement of ultra-high thickness ICs. Be that as it may, because of ceaseless scaling down, a circumstance has been achieved, where the execution parameters of the MOSFETs are corrupted (due to the fundamental physical cutoff points), to the degree that it is exceptionally hard to create ICs with nano-scale mass MOSFETs. Another age gadget, which can offer great execution parameters i.e., low power utilization and fast, notwithstanding for nano-scale gadgets, is required.

VII. FUTURE SCOPE

The SOI is a marvelous discovery in the field of microelectronics and a breakthrough technology with a robust future. It's an innovation that will allow the semiconductor industry to continue to deliver an even better experience for consumers on next-generation digital devices.SOI will enable the device to operate faster. It is a simpler way to deliver these benefits compared to other alternatives and is available for design and manufacturing today.

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