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The Approach on Influence of Biasing Circuit in Wideband Low Noise Amplifier to Evaluate Robustness Performance

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***Abstract*—This proposed work investigates the effects of biasing circuit in the ultra-wideband microwave low noise amplifier which operates between 3GHz to 10GHz. The complete circuit is visualized the importance of every component in the design with respect to linear measurements like Gain, Noise Figure, Return loss under unconditionally stable condition. The design and realization are made by using Hybrid Microwave integrated circuit in AWR microwave office. The thing that is absolutely necessary and frequently the difficult step in the design of an LNA is 'biasing circuit design'. The difficulty situation arises because traditional methods LNA by using S-parameters data files in EDA tools provides almost all linear measurements. Hence a number of time consuming iterations of different biasing circuits with optimization methods may be required to reach targeted specifications with the fixed operating point at the desired points in the load line. Considering this behavior, various alternate biasing circuit schemes are prepared and founded the results associated with it. Furthermore, this paper unmistakably clarifies the impacts of the biasing circuit by utilizing intermodulation and harmonics distortion technique for portrayal characterization. Different cases and sorts of the biasing circuits with various biasing focuses have been tested and given clear perspective of the biasing ideas.**

Keywords- PHEMT, Biasing Networks, AWR microwave office, Impedance matching, HMIC and LNA

I. INTRODUCTION

Advancing in the wireless communication networks it has been arise the set of circumstances found that design of Microwave circuits should meet various parameters at a time with good performance. In case of LNA the parameters like Bandwidth, Gain, Noise figure and return loss should all meet the specifications at the same time eventually all those parameters with not work with each other favors. To meet at the specifications with the help of theoretical equations and majorly the tuners in the commercial software EDA tools like AWR Microwave office, ADS, HFSS etc. are made quite easier for microwave circuit designing.

[5] In contrast, hybrid MIC circuits using discrete components and distributed elements occupy more area and dissipate more power. However, hybrid MIC technologies provide a shorter design time, capabilities of customization and fine tune of fabricated circuits. Also, Optimization of the variables becomes quite easy.

In this paper, authors present effects of biasing in the LNA which includes design optimization and analysis of matching networks and various bias circuits and variation of their effects in primary circuit are explained. [6] To satisfy high gain, LNA is designed by using cascade topology and to achieve maximum power transfer, impedance matching is essential for proper gain and NF with VSWR. Some of network to build impedance matching uses lump element, micro strip line or combination of such elements. Many design of LNA have been conducted and proposed to satisfy high gain and good impedances matching network using lump element or micro strip line and some of characteristic design has been obtained at the defined frequency and application. For all circuit design the industrial standard AWR microwave office tool is used, also to optimize micro strip line and impedance matching to determine trade off value of gain, Noise Figure, return loss and voltage standing wave ratio (VSWR).

This paper is organized as follows. The research background which is composed of recently published articles with respect to biasing circuits in microwave is described in Section II, the design of the low-noise amplifier with different bias circuit is presented in Section III, the LNA performance under limited set exposures with results are discussed in Section IV and finally the conclusive remarks are drawn in the last section.

II. RESEARCH BACKGROUND

This segment examines distributed data about biasing circuit in microwave circuits, additionally, their estimations techniques and investigation. [7] In their work, presented a balun low noise amplifier (LNA) in which the noise figure (NF) and power consumption are reduced by using a feedback

biasing structure. The circuit was based on a conventional wideband balun LNA with noise cancellation. In which they replaced the typical current source of the CG stage by a transistor that established a feedback loop in that stage. [8] introduced linearity change of a 10 W GaN HEMT PA utilizing a dynamic entryway biasing procedure for smoothing an exchange period of the PA as indicated by the quick information power. Zhang, Ma, Yu, & Li, [9], exhibited a dynamic biasing circuit was inserted in the chip which mitigates the deviation of biasing point, enhances the solidness and consistency of execution. Both noise and small signal measurements are performed on-wafer. Ghosh & Srivastava, [10] , gave the symmetric design biasing system, which makes the structure polarization uncaring not at all like which was accounted for active frequency-selective surface(AFSS). Harzheim, Heuermann, & M. Marso,[11], displayed a versatile biasing strategy for step recuperation diode based brush generators which was controlled by a product schedule. The point was to give the most extreme conceivable consonant yield power for a given arrangement and diverse information frequencies amid info power variety.

A. Hypothesis behind the Biasing Circuits

With the thought of practical bias ways for inclination of transistors. Contrasted with design practice at lower frequencies, fitting biasing expressions are more constrained RF and microwave since it is hard to keep the biasing circuit's parasitic from connecting with the signal path way at microwave frequencies [12-14].

B. Bias Circuits and its Instabilities

Once the microwave LNA is composed, it stays to give the dc bias voltages and currents required for the dynamic active device. This is no straightforward issue, as the courses of action to present the biases can aggravate the microwave circuit. By and large, high impedance miniaturized micro strip follows can be utilized as decoupling inductors, yet alert must be practiced not to make a low frequency oscillator circuit in the predisposition bias network system.

A typical reason for inconvenience is the utilization of an inductor with a huge bypass capacitor, which can make a resonator in the GHz region that can bolster oscillation of the active components, which will have high gain at lower frequencies.

Bias-circuit instabilities are a common source of problems in amplifiers and other active circuits. These for the most part result from the utilization of inductors and capacitors in the Bias-circuit without respect to resonances or circumstances where 180° stage movement can happen.

III. LNA DESIGN AND ANALYSIS

LNA parameters are mainly depend on S parameters which varies with respect to frequency. Also Γin depends on Zin and Γ_L, Γ_L depends on Z_L and Γ_{IN} . Zin and Z_L will be different for different biasing components. Effects of biasing components is also frequency dependent.

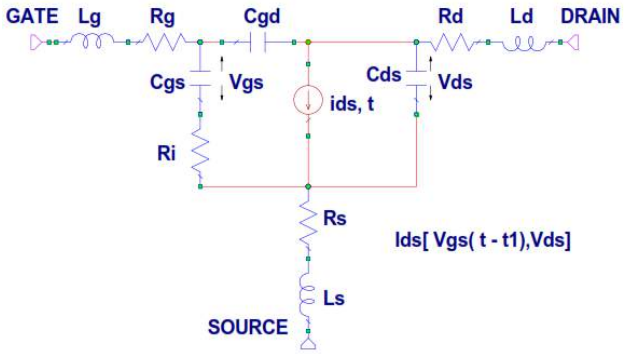

Figure 1. The small signal model of a pHEMT

Cgs and Cgd depends on the biasing voltage because the depletion region changes with the bias .

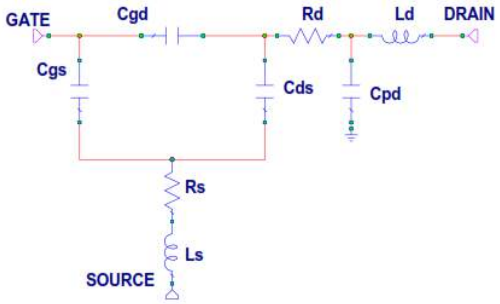

Figure 2. The small signal model of a pHEMT at zero drain bias and gate voltage below pinch-off

The three capacitances Cg, Cs and Cd are given by triangle-star transformation as given below

$C_g = C_{gs} + C_{gd} + [(C_{gs} * C_{gd})/ C_{ds}]$ (1)
$C_s = C_{gs} + C_{ds} + [(C_{gs} * C_{ds})/ C_{gd}]$ (2)
$C_d = C_{ds} + C_{gd} + [(C_{gd} * C_{ds})/ C_{gs}]$ (3)

Input port and output port impedances can be expressed using

$Z_{11} = R_g + R_s + j * [\omega(L_g + L_s) – (1/ \omega) \{ (1/C_g)+ (1/C_s)\}]$ (4)
$Z_{22} = R_d + R_s + j * [\omega(L_d + L_s) – (1/ \omega) \{ (1/C_d)+ (1/C_s)\}]$ (5)

Input reflection coefficient and output reflection coefficient

$\Gamma_{in} = (Z_{in} – Z_0)/(Z_{in} + Z_0)$ (6)
$\Gamma_L = (Z_L – Z_0)/(Z_L + Z_0)$ (7)

Equivalent input and output impedances can be expressed in terms of two port Z parameters.

$Z_{in} = Z_{11} – [(Z_{12} * Z_{21})/(Z_L + Z_{22})]$ (8)
$Z_L = Z_{22} – [(Z_{12} * Z_{21})/(Z_G + Z_{11})]$ (9)

On the premise of the above arrangement numerical conditions unmistakably reliance of Γin and ΓL furthermore Zin and ZL on Cg, Cs and Cd which changes because of progress in biasing conditions.

A. Case 1: With Ideal Bias

Case 1 which incorporates the circuit schematic in figure 3 arranged by using the S-Parameters .S2P documents or mdiff

files of the transistor ATF36163 from Avago technologies. For the simulations and results got depend on the S-parameters investigation without real biasing circuit (real circuit on PCB format). For this case the matching circuit has been set up to accomplish most ideal consequences of the general circuit regarding GAIN, NF, RL for the total bandwidth from 3-10GHz

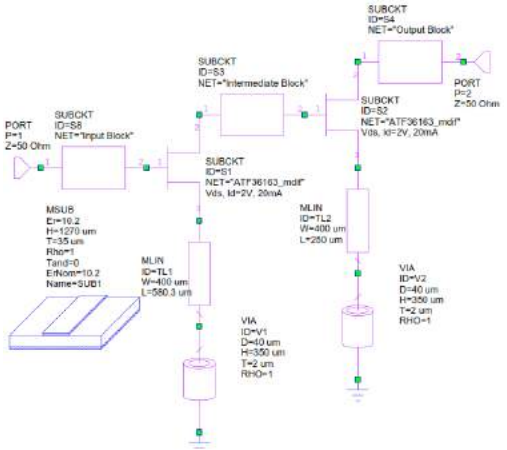

Figure 3. Complete Block

The above figure 3 is of the complete block of the circuit in which it is comprised of three sub blocks called "Input Block" which is displayed in figure 4 in detail, "Intermediate Block" figure 5 and "output block" figure 6. All this blocks are prepared for the best possible results to make transistor to behave has LNA.

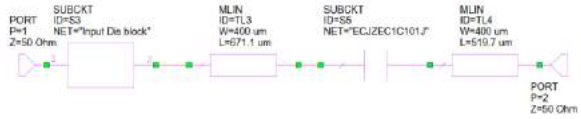

Figure 4. Input Block

The "input block" which is intended for the input matching and mainly it consists of capacitor and one more sub block called "Input Dis Block" which is appeared in figure 7.

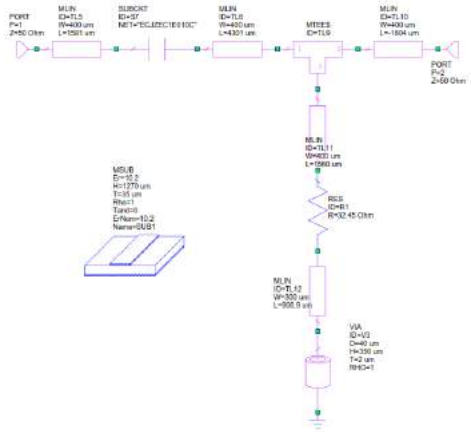

Figure 5. Intermediate Block

The above block figure 5 is designed for intermediate matching between two transistors in cascaded topology.

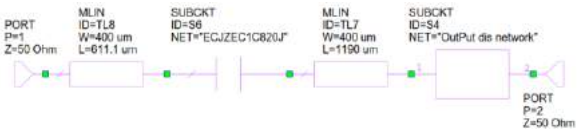

Figure 6. Output Block

The "Output block" figure 6 which is intended for the output matching and mainly it consists of capacitor and one more sub block called "Output Dis Block" which is appeared in figure 8.

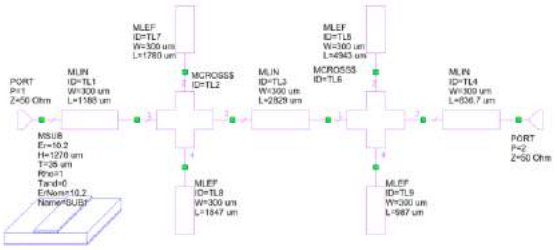

Figure 7. Input Dis block

There are two sub blocks called "Input Dis Block" figure 7 and "Output Dis Block" figure 8 are set up by utilizing just microstrip lines to give great return loss performances at input and output.

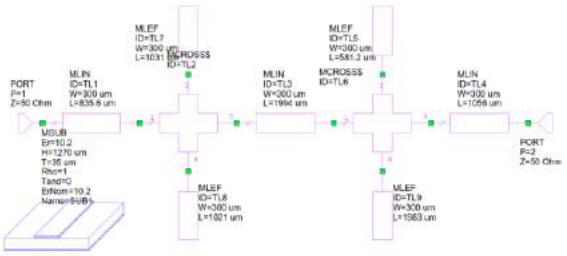

Figure 8. Output Dis network

Case 1 which incorporates the circuit schematic in figure () arranged by using the S-Parameters .S2P documents or mdiff files of the transistor ATF36163 from Avago technologies. For the simulations and results got depend on the S-parameters investigation without real biasing circuit (real circuit on PCB format). For this case the matching circuit has been set up to accomplish most ideal consequences of the general circuit regarding GAIN, NF, RL for the total bandwidth from 3-10GHz.

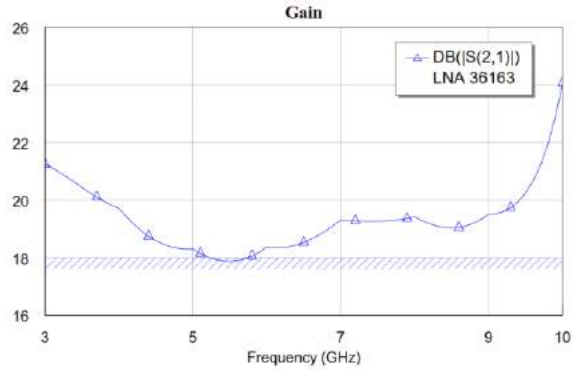

Figure 9. Transducer Gain response over 3-10GHz for the Ideal bias Circuit.

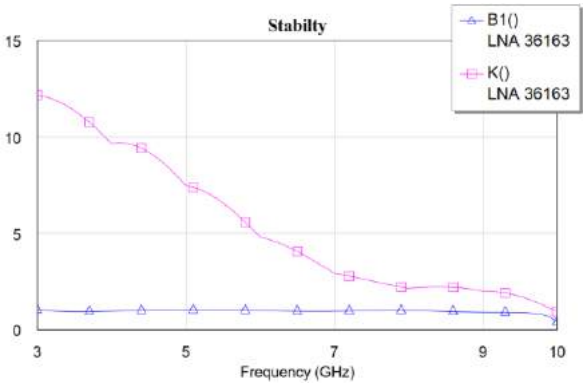

Figure 10. Stability Factors response over 3-10GHz for the Ideal bias Circuit.

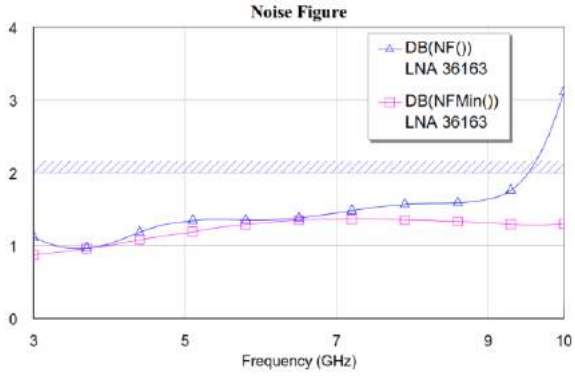

Figure 11. Noise Factors response over 3-10GHz for the Ideal bias Circuit

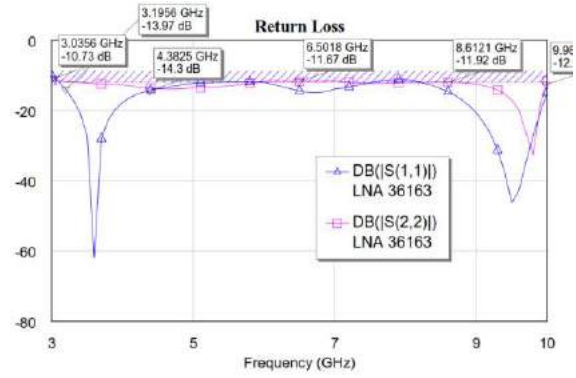

Figure 12. Return Loss response over 3-10GHz for the Ideal bias Circuit

The above simulation results found from the case 1 schematic which is improved to most ideal results concerning return loss satisfying not exactly - 10dB with the acquire gain more than 18dB and Noise figure under 2dB.

TABLE I. CHANGE IN LNA PARAMETERS WITH RESPECT TO VARIATION IN IDEAL BIAS POINTS

Band width	Bias Points (VDS, ID)	Gain in dB	Noise Figure in dB	Return Loss (S11, S22) in dB
3-10	1.5V, 10mA	17-20.5	<1.5	<-11 , <-12
3-10	1.5V, 15mA	17.5-20.8	<1.5	<-11.5, <-13
3-10	1.5V, 20mA	17.7-20.9	<1.6	<-11.5, <-13
3-10	2V, 10mA	17.4-20.7	<1.531	<-10.5, <-12
3-10	2V, 15mA	17.7-21	<1.5	<-11, <-12
3-10	2V, 20mA	17.9-21.21	<1.6	<-11, <-13

The above table portrays the vigour, robustness of the designed circuit, for the varieties of the bias points which has influenced immaterial changes in the Gain, Noise figure and return loss which is plainly depicted in the table.

B. Case 2: with inductive drain bias and resistive gate bias

For this situation, the biasing circuits are built to a similar circuit which is utilized as a part of case 1 which is inductive drain and resistive bias. Microwave Inductors are used has biasing circuit at Drain as showed up in the above Figure(?). They give high Impedance at designed band frequencies in this way it won't usually give up transducer GAIN. In any case, the biasing circuits will reliably have their resonances. It is essential to plan and enhance the entire LNA design circuit with Inductor equivalent circuit show in order to anticipate the circuit execution is to be exactly.

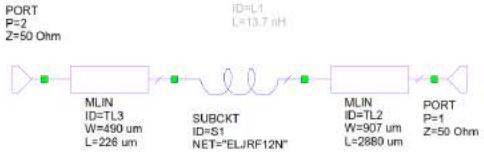

Figure 13. Drain Bias with Inductor

Figure 14. Gate Bias with resistor

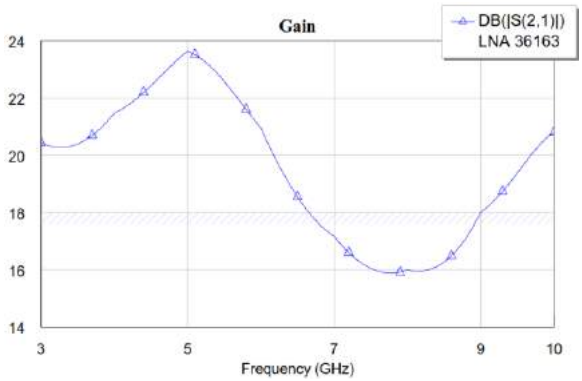

Figure 15. Transducer Gain response over 3-10GHz for the inductive drain bias and resistive gate bias circuit.

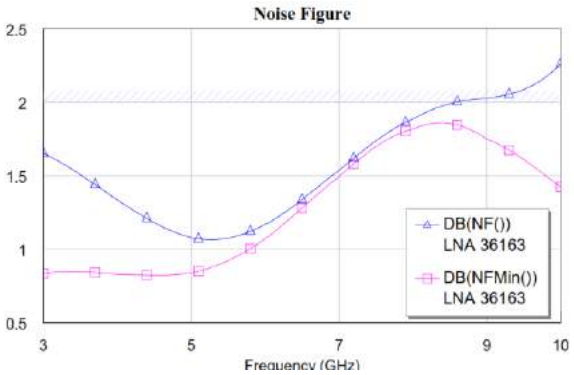

Figure 16. Noise Factors response over 3-10GHz for the inductive drain bias and resistive gate bias circuit.

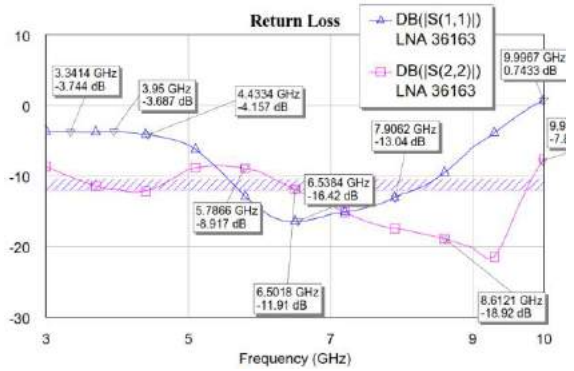

Figure 17. Return Loss response over 3-10GHz for the inductive drain bias and resistive gate bias circuit

For the same designed circuit for the case 1, by only expansion of the inductive drain and resistive gate bias circuit to has made its own resonance and carried variety of the outcome as for frequency and obviously appeared in the above figures.

TABLE II. CHANGE IN LNA PARAMETERS WITH RESPECT TO VARIATION OF BIAS POINTS FOR INDUCTIVE DRAIN AND RESISTIVE GATE BIAS

Band width	Bias Points (V_{DS}, I_D)	Gain in dB	Noise Figure in dB	S11 in dB	S22) in dB
3-10	1.5V, 10mA	15.5-23	<1.5	< (-3 to -15)	< (-9 to -20)
3-10	1.5V, 15mA	15.9-23.2	<1.5	< (-3.5to -15.7)	< (-9 to -18)
3-10	1.5V, 20mA	16-23.2	<1.6	< (-3.6 to -16)	< (-9 to -22.5)
3-10	2V, 10mA	15.5-23.4	<1.5	<(-3.6 to -15)	< (-9 to -20)
3-10	2V, 15mA	15.81-23.5	<1.5	<(-3.6 to -16)	< (-9 to -21)
3-10	2V, 20mA	15.92-23.62	<1.6	<(-3.7 to -16)	< (-9 to -21)

By the insertion of the inductive drain and resistive gate bias circuit the gain has diminished by 2dB and gain flatness additionally got aggravated. Because of resistive gate bias Noise figure got expanded to 2dB and discovered return loss some enormous variations and it has been found the circuit bandwidth has decreased to 3-9GHz.

C. Case 3: with single pair LC

In this case, biasing circuit is prepared using a set of inductor and capacitor at both drain and gate side. Each extra Inductance with parasitic (resistance, capacitance) in arrangement with the capacitor grounded, whether of parasitic source" inside" the capacitor brought about by design or development, diminishes the adequacy of the bias circuit. The pair of LC circuits creates its own resonance and disturbs LNA parameters. Long connections between the capacitor and ground are extra undesirable arrangement inductance – regardless of to whether the inductance originates from the interfacing legs of the capacitor, the conductor tracks or dashes on the component group installation. Designers and layout specialists are regularly confronted with apparently practically insoluble issues in such manner, as limitations, for example, the space accessibility inside the component group and so on.

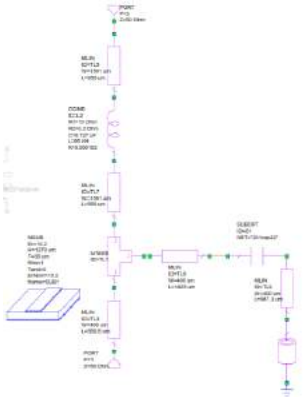

Figure 18. Drain Bias

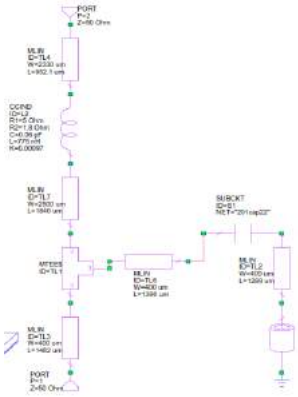

Figure 19. Gate Bias

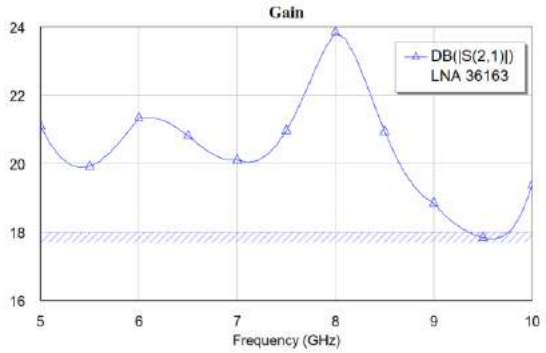

Figure 20. Gain response over 5-10GHz for the single pair LC bias circuit

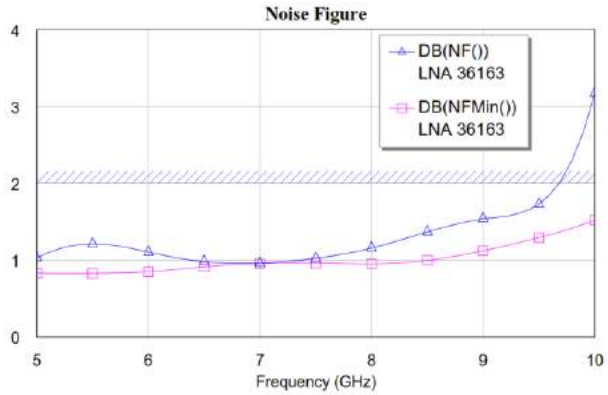

Figure 21. Noise Figure response over 5-10GHz for the single pair LC bias circuit

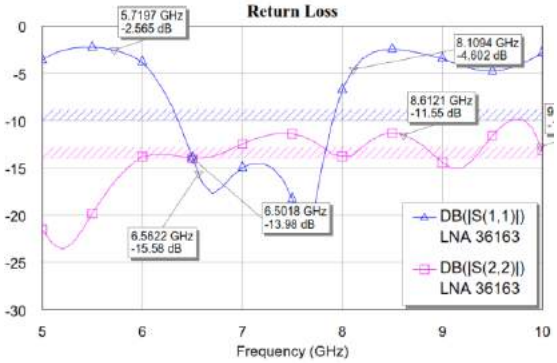

Figure 22. Return Loss response over 5-10GHz for the single pair LC bias circuit

the above simulated results are from case 3 circuit which has not affected gain or noise figure but created the resonance and disturbed the input return loss in its own band between 6-8GHz.

TABLE III. CHANGE IN LNA PARAMETERS WITH RESPECT TO VARIATION OF BIAS POINTS FOR LC BIASING CIRCUIT

Band width	Bias Points (VDS(V), ID(MA))	Gain in dB	Noise Figure in dB	S11 in dB	S22) in dB
3-10	1.5, 10	16.8-23	<1.5	< -2.8 to -20	< -11 to -20
3-10	1.5, 15	17.5-23	<1.5	< -2.7 to -20	< -11 to -23
3-10	1.5, 20	17.7-23	<1.5	< -2.6 to -22	< -11 to -23
3-10	2, 10	17-23.5	<1.4	<-2.7 to -20	< -11 to -23
3-10	2, 15	17.5-23.7	<1.4	<-2.6 to -21	< -11 to -23
3-10	2, 20	17.8-23.7	<1.4	<-2.6 to -21	< -11 to -23

the above table describes the variations of the parameters with respect to the different biasing points. It is observed the best result found for this case at bias point 2V, 20mA.

D. Case 4: with double pair LC

In this case 4 which is designed for the same case 1 circuit by adding double pair LC at both drain and gate of the transistors. This case is prepared to show the double LC pair will creates its own resonance with increase in the bandwidth. Only biasing circuit will be optimized to best result possible.

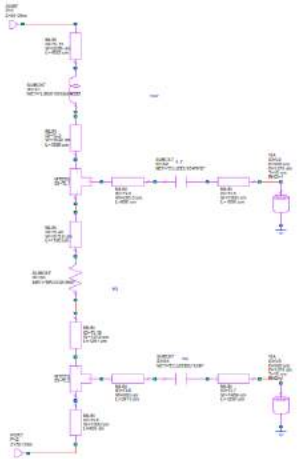

Figure 23. Drain Bias

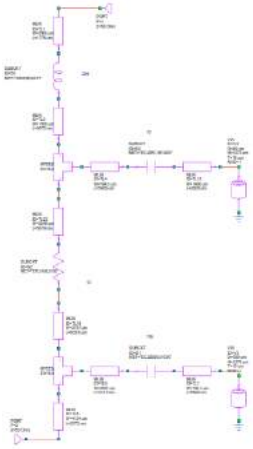

Figure 24. Gate Bias

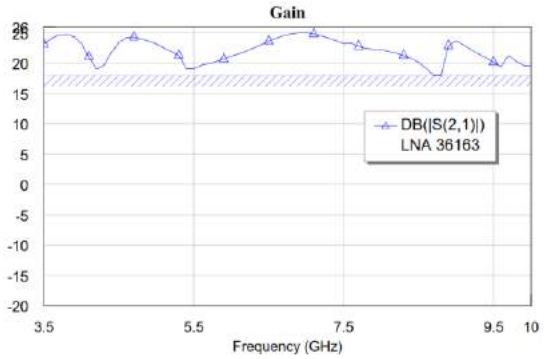

Figure 25. Gain response over 3.5-10GHz for the double pair LC bias circuit

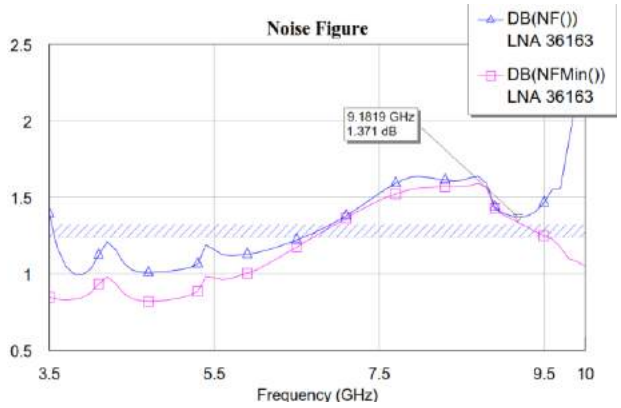

Figure 26. Noise Figure response over 3.5-10GHz for the double pair LC bias circuit

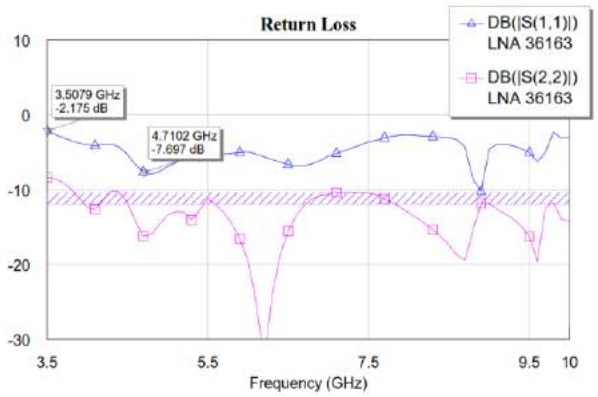

Figure 27. Return Loss response over 3.5-10GHz for the double pair LC bias circuit

By using double pair LC as biasing circuit has improved gain and input return loss with minor increase of noise figure.

TABLE IV. CHANGE IN LNA PARAMETERS WITH RESPECT TO VARIATION OF BIAS POINTS FOR DOUBLE BIASING CIRCUITS

Band width	Bias Points (VDS(V), ID(MA))	Gain in dB	Noise Figure in dB	S11 in dB	S22) in dB
3-10	1.5, 10	16.8-23	<1.6	< -1.7 to -10	< -9 to -20
3-10	1.5, 15	17.5-23	<1.6	< -1.8 to -10	< -9 to -20
3-10	1.5, 20	17.7-23	<1.6	< -2 to -10	< -9 to -20
3-10	2, 10	17-23.5	<1.6	< -2 to -10	< -9 to -20
3-10	2, 15	17.5-23.7	<1.5	< -2 to -10	< -9 to -20
3-10	2, 20	17.8-23.7	<1.6	< -2 to -10	< -9 to -20

IV. BIASING CIRCUIT EFFECTS ON NON-LINEAR CHARACTERISTICS

In this section, illustrations and clarifications of LNA Design Circuit as for biasing Circuit will be given. [15-16] The effects of Biasing circuit are explained by insertion of single tone sinusoidal voltage wave (V sin(ωt)) to the non-signal voltage results in

$v_{gs} = V_{GSQ} + V \sin(\omega t)$

vgs will be the function of Vds and Id biasing point of the transistor which has already been tabulated for the multiple cases and discussed. Then the harmonic distortion KF is

$$KF = \frac{Relative\ value\ of\ second\ harmonics}{Relative\ value\ of\ fundamental\ harmonics} \quad (10)$$

$$KF = \frac{V}{4(Vgs - Vp)} \quad (11)$$

Where V is maximum amplitude of the signal.

Noted: Distortion Factor approaches to its minimum as Vgs tends to 0

Cross modulation (Intermodulation) produced when two sine wave signals are amplified at the same time.

$v_{gs} = V_{GSQ} + V_1 \sin(\omega t) + V_2 \sin(\omega t)$ (12)

Since the output current includes the sum and difference components of the two sinusoidal waves in which intermodulation results in

$$IM = \frac{Relative\ value\ of\ cross\ modulation\ components}{Relative\ value\ of\ fundamental\ harmonics}$$

$$IM = \frac{V_1 * V_2}{\sqrt{2}(V_{GSQ} - V_p)(\sqrt{V_1^2 + V_2^2}} \quad (13)$$

In this case, also it has been clearly examined that distortion factor decreases as bias is brought closer to V_{GSQ}=0. These two-distortion factor will exist in biased circuit which will deteriorate performance of the designed circuit.

V. SUMMARY

The experimented results of this work can be summarized as following in the preferences of cases:

Case1: Ideal Bias LNA circuit intended for the best reasonable estimations of Gain, NF and Bandwidth (3-10GHz) which is utilized to correlate for the remaining three biasing strategies likely Drain Inductance and gate resistance bias, LC bias and double LC bias.

Case 2: Drain Inductance and gate resistance bias is recommended for the LNA design whose bandwidth is up to 4GHz. The performance in this case linearly Gain decrease and NF increases and stability will not be affected at any cost.

Case 3: LC bias is suggested for the LNA design for the smaller bandwidth generally around 2GHz. The LNA performance with respect to Gain and NF will be great and results will keep up flatness over small bandwidth.

Case 4: Double LC is proposed for the wideband and ultra-band with the viable cost on return loss, Gain and NF won't be highly influenced.

A. Confinement of the Biasing Circuit Design

1) the main cause of the distortion or the variations of the results with various cases of the biasing circuit is the non-linearity in the transfer characteristics of the overall circuit with micro strip line

2) Distortion is also caused by the output conductance gd related to operating point and drain voltage Vds.

B. Conceivable Solution

1) By applying the feedback to the circuit both distortion factor and bandwidth can be improved.

2) It is possible to have wideband amplifier with low distortion factor by initially designing the amplifier for the high gain and tuning the gain to its optimum level by using feedback.

VI. CONCLUSION

In this work the effect of biasing circuit on LNA performance. The effect of three different biasing strategies, namely; Drain Inductance and gate resistance bias, LC bias and double LC bias are compared with the ideal bias characteristics of the LNA design. The parameters in each of these approached are re-enacted, Simulated and optimized in AWR microwave office. The importance of the biasing techniques as far as bandwidth, Noise Figure, Gain and return Loss. Every case has been breaking down with criticalness of the segments utilized as a part of analysis in component level of the design and corresponding impacts on overall circuit have been introduced. This work is expected to contribute in LNAs for satellite communications transmissions, Wi-Fi devices and weather radar systems.

The proposed work given examination, comparison of different biasing techniques and also clarified with small signal equivalent circuit model. Moreover, it is obviously presumed that LNA performances is altogether influenced by the biasing circuit strategies. The authors are extended their clear reasonable view and summarized about the effects of different biasing strategies as for BW, Gain and NF.

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